REMARKS

Claim 1 has been amended. Claims 1 to 24 remain active in this application of which claims 15 to 17 and 22 have been indicated to be allowable.

Claims 1 to 14 and 18 to 21, 23, and 24 were rejected under 35 U.S.C. 103(a) as being unpatentable over Galton et al. (U.S. 6,697,004) in view of Chen (U.S. 6,710,720 and Ruha et al. (U.S. 6,473,019). The rejection is respectfully traversed.

Claim 1 requires, among other features, an analog-to-digital conversion system, having a noise shaping system with respect to quantization noise associated with said converter of an order N having less than N integrator amplifiers, the noise shaping system being coupled to the first A/D converter and providing the first analog feedback signal according to the first digital output, the first analog feedback signal being noise shaped by the noise shaping system to an order N with respect to a quantization error associated with the first A/D converter, wherein N is an integer greater than 1. No such feature is taught or suggested by Galton et al., Chan or Ruha et al. either alone or in the combination as claimed. Note in Fig. 7 of Galton et al., the figure cited by the examiner, that there are two integrators 704 and 708 in the second order conversion system therein. Note also in Chan at column 5, lines 18 and 19 that it is stated that "[t]he number of integrators in the modulator is generally referred to as the order of the modulator". All of the applied references have a number of integrators equal to the order of the modulator depicted therein or do not indicate anything to the contrary.

Claim 2 to 14 depend from claim 1 and therefore define patentably over the applied references for at least the reasons presented above with reference to claim 1.

In addition, claim 2 further limits claim 1 by requiring that N = 2. No such combination is taught or suggested by Galton et al., Chan or Ruha et al.

Claim 3 further limits claim 2 by requiring that the first A/D converter be a flash analog-to-digital converter. No such combination is taught or suggested by Galton et al., Chan or Ruha et al.

Claim 4 further limits claim 2 by requiring that the first A/D converter be a flash ADC providing a thermometer coded first digital output representative of the system analog input. No such combination is taught or suggested by Galton et al., Chan or Ruha et al.

Claim 5 further limits claim 2 by requiring a digital decimation filter coupled with the first A/D converter and providing a multi-bit digital output according to the first digital output, the multi-bit digital output being representative of the system analog input. No such combination is taught or suggested by Galton et al., Chan or Ruha et al.

Claim 6 further limits claim 2 by requiring that the noise shaping system comprise a first DAC coupled with the first A/D converter, the first DAC providing an analog first DAC output according to the first digital output and a delta sigma modulator coupled with the first DAC, the delta sigma modulator providing a second digital output according to a difference between the first DAC output and the system analog input. No such structure is taught or suggested by Galton et al, Chen, Ruha et al. or any proper combination of these references either alone or in the combination as claimed.

Claim 6 further requires a digital error feedback system coupled with the delta sigma modulator, the digital error feedback system providing the first analog feedback signal to the first A/D converter according to the second digital output, the first analog

feedback signal being noise shaped by the digital error feedback system to order N with respect to a quantization error associated with the delta sigma modulator. No such structure is taught or suggested by Galton et al, Chen, Ruha et al. or any proper combination of these references either alone or in the combination as claimed.

Claim 7 further limits claim 6 by requiring that the delta sigma modulator comprise an integrator of order N-1 coupled with the first DAC, the integrator providing an analog integrator output according to the first DAC output, according to the system analog input, according to the first analog feedback signal, and according to an analog modulator feedback signal, the integrator having less than N integrator amplifiers, a second A/D converter coupled with the integrator, the second A/D converter providing a second digital output according to the integrator output and a second DAC coupled with the second A/D converter, the second DAC providing the modulator feedback signal to the integrator according to the second digital output, the integrator output being noise shaped by the integrator to an order N-1 with respect to a quantization error associated with the second A/D converter. No such structure is taught or suggested by Galton et al, Chen, Ruha et al. or any proper combination of these references either alone or in the combination as claimed.

Claim 8 further limits claim 7 by requiring that the noise shaping system further comprises an analog delay system coupled with the integrator and with the first A/D converter, the analog delay system providing an analog delayed integrator output signal to the integrator and to the first A/D converter. No such structure is taught or suggested by Galton et al, Chen, Ruha et al. or any proper combination of these references either alone or in the combination as claimed.

Claim 9 further limits claim 7 by requiring that wherein the digital error feedback system comprise a digital signal processing system coupled with the delta sigma modulator, the digital signal processing system providing a third digital output according to the second digital output, the third digital output being noise shaped by the digital signal processing system to order N with respect to a quantization error associated with the delta sigma modulator and a third DAC coupled with the digital signal processing system, the third DAC providing the first analog feedback signal to the first A/D converter according to the third digital output. No such structure is taught or suggested by Galton et al, Chen, Ruha et al. or any proper combination of these references either alone or in the combination as claimed.

Claim 10 further limits claim 9 by requiring that at least one of the first DAC, the second DAC, and the third DAC comprises a switched capacitor system comprising a plurality of selectable capacitors providing an analog output corresponding to a digital input code using DAC elements selected according to the digital input code and a dynamic element matching system coupled with the switched capacitor system, wherein the dynamic element matching system varies the selection of capacitors. No such structure is taught or suggested by Galton et al, Chen, Ruha et al. or any proper combination of these references either alone or in the combination as claimed.

Claim 11 further limits claim 6 by requiring that the digital error feedback system comprises a digital signal processing system coupled with the delta sigma modulator, the digital signal processing system providing a third digital output according to the second digital output, the third digital output being noise shaped by the digital signal processing system to order N with respect to a quantization error associated with the delta sigma

modulator and a third DAC coupled with the digital signal processing system, the third DAC providing the first analog feedback signal to the first A/D converter according to the third digital output. No such structure is taught or suggested by Galton et al, Chen, Ruha et al. or any proper combination of these references either alone or in the combination as claimed.

Claim 12 further limits claim 1 by requiring that the noise shaping system include a first DAC coupled with the first A/D converter, the first DAC providing an analog first DAC output according to the first digital output, a delta sigma modulator coupled with the first DAC, the delta sigma modulator providing a second digital output according to a difference between the first DAC output and the system analog input and a digital error feedback system coupled with the delta sigma modulator, the digital error feedback system providing the first analog feedback signal to the first A/D converter according to the second digital output, the first analog feedback signal being noise shaped by the digital error feedback system to order N with respect to a quantization error associated with the delta sigma modulator. No such combination is taught or suggested by Galton et al., Chan or Ruha et al.

Claim 13 further limits claim 12 by requiring that the delta sigma modulator include an integrator of order N-1 coupled with the first DAC, the integrator providing an analog integrator output according to the first DAC output, according to the system analog input, according to the first analog feedback signal, and according to an analog modulator feedback signal, the integrator having less than N integrator amplifiers, a second A/D converter coupled with the integrator, the second A/D converter providing a second digital output according to the integrator output and a second DAC coupled with

the second A/D converter, the second DAC providing the modulator feedback signal to the integrator according to the second digital output, wherein the integrator output is noise shaped by the integrator to an order N-1 with respect to a quantization error associated with the second A/D converter. No such combination is taught or suggested by Galton et al., Chan or Ruha et al. either alone or in the combination as claimed.

Claim 14 further limits claim 13 by requiring that the noise shaping system further include an analog delay system coupled with the integrator and with the first A/D converter, the analog delay system providing an analog delayed integrator output signal to the integrator and to the first A/D converter. No such combination is taught or suggested by Galton et al., Chan or Ruha et al. either alone or in the combination as claimed.

Claim 18 requires, among other features, a first DAC coupled with the first A/D converter, the first DAC providing an analog first DAC output according to a first digital output and a delta sigma modulator coupled with the first DAC, the delta sigma modulator providing a second digital output according to a difference between the first DAC output and a system analog input. No such combination of elements is taught or even remotely suggested by Fig. 7 of Galton et al. as demonstrated in the prior response. No such structure is found in Chen or Ruha et al. either alone or in any proper combination of these references and no such showing has been made in the Office action.

Claim 18 further requires a digital error feedback system coupled with the delta sigma modulator, the digital error feedback system providing the first analog feedback signal to the first A/D converter according to the second digital output. No such structure

is taught or suggested by Galton et al., Chen or Ruha et al. or any proper combination of these references either alone or in the combination as claimed.

In the event the rejection is repeated, it is requested that a showing be made as to how the examiner proposed to have this claim readable on any one or proper combination of these references.

Claims 19 to 21 depend from claim 18 and therefore define patentably over the applied references for at least the reasons presented above with reference to claim 18.

In addition, claim 19 further limits claim 18 by requiring that the delta sigma modulator comprise less than N integrator amplifiers, and wherein the first analog feedback signal is noise shaped to order N with respect to a quantization error associated with the first A/D converter, wherein N is an integer greater than 1. No such structure is taught or suggested by Galton et al., Chen, Ruha et al. or any proper combination of these references either alone or in the combination as claimed.

Claim 20 further limits claim 18 by requiring that the delta sigma modulator comprises an integrator coupled with the first DAC, the integrator providing an analog integrator output according to the first DAC output, according to the system analog input, according to the first analog feedback signal, and according to an analog modulator feedback signal, the integrator having N-1 integrator amplifiers. No such structure is taught or suggested by Galton et al., Chen, Ruha et al. or any proper combination of these references either alone or in the combination as claimed.

Claim 20 further requires a second A/D converter coupled with the integrator, the second A/D converter providing a second digital output according to the integrator

output. No such structure is taught or suggested by Galton et al., Chen or Ruha et al. or any proper combination of these references either alone or in the combination as claimed.

Claim 20 yet further requires a second DAC coupled with the second A/D converter, the second DAC providing the modulator feedback signal to the integrator according to the second digital output. No such structure is taught or suggested by Galton et al., Chen, Ruha et al. or any proper combination of these references either alone or in the combination as claimed.

Claim 20 even further requires that the integrator output be noise shaped by the integrator to an order N-1 with respect to a quantization error associated with the second A/D converter. No such structure is taught or suggested by Galton et al., Chen, Ruha et al. or any proper combination of these references either alone or in the combination as claimed.

Claim 21 further limits claim 20 by requiring that the noise shaping system further comprise an analog delay system coupled with the integrator and with the first A/D converter, the analog delay system providing an analog delayed integrator output signal to the integrator and to the first A/D converter. No such structure is taught or suggested by Galton et al., Chen, Ruha et al. or any proper combination of these references either alone or in the combination as claimed.

Claim 23 requires, among other features, a noise shaping system of an order N for providing a noise shaped analog feedback signal to a first A/D converter in an analog-to-digital conversion system which includes a second A/D converter coupled with the DAC, the second A/D converter comprising less than N integrator amplifiers and providing a second digital output according to a difference between the DAC output and a system

analog input, N being an integer greater than 1. The argument presented above with reference to claim 1 applies as well to this claim since Chen and Ruha et al. fail to overcome the deficiencies in Galton et al. as noted above with reference to claim 1.

Claim 24 requires, among other features, a second order noise shaping system for providing a noise shaped analog feedback signal to an A/D converter in an analog-to-digital conversion system having not more than or less than one first order integrator having a single amplifier. No such structure is taught or suggested by Galton et al, Chen, Ruha et al. or any proper combination of these references either alone or in the combination as claimed.

In view of the above remarks, favorable reconsideration and allowance are respectfully requested.

Respectfully submitted,

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